Hysteresis control for a grid connected dual-buck inverter
Control por histéresis para un inversor buck-dual conectado a la red

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Abstract

Single-phase inverters are widely used in different renewable energy applications. Although the full-bridge inverter is typically used, dual-buck inverters provide an important advantage, since they eliminate the shoot-through problems. However, solutions proposed in the literature require additional inductors, use linear controllers designed around an operation point, or cannot be used in grid-connected applications. This paper presents a hysteresis current control of a single-phase dual-buck full-bridge inverter for grid-connected active power injection. Includes the dynamical model in state variables, as well as analytical conditions to guarantee the evolution of the error dynamics in a set with boundaries defined by the designer. Moreover, the paper provides guidelines for the design of the dead band required for the transitions between the positive and negative semi-cycles (and vice-versa) of the grid voltage. Finally, simulation results validate the main features of the controller as well as the design of the dead band.

Keywords: dual-buck; microinverter; active power; hysteresis control.

Resumen

Los inversores monofásicos son ampliamente usados en diferentes aplicaciones de energías renovables. Aunque típicamente se usa el inversor de puente completo, el inversor buck-dual provee una ventaja importante porque elimina el problema de posibles cortos-circuitos. Sin embargo, las soluciones reportadas en la literatura requieren inductores adicionales, usan controladores lineales diseñados para un punto de operación, o no se pueden usar en aplicaciones de conexión a la red. En este artículo se presenta un control por histéresis para un inversor monofásico buck-dual de puente completo con conexión a la red para inyección de corriente activa. En particular, se presenta el modelo matemático en variables de estado y se obtienen condiciones analíticas para garantizar la evolución de la dinámica de error dentro de un conjunto con límites establecido por el diseñador. Además, se discuten los elementos para diseñar la banda muerta requerida en la transición entre los semi-ciclos positivos y negativos de la tensión de la red. Finalmente, los resultados de simulación validan las principales características del controlador propuesto, así como el diseño de la banda muerta.

Palabras clave: buck-dual; microinversor; potencia activa; control por histéresis.

1. Introducción

Recently, renewable energy sources as photovoltaic generators, wind turbines, and energy storage systems have been continuously growing, becoming a cost-effective alternative to supply the demand of the market while diversifying the energy matrices and reducing the environmental impact of energy generation [1, 2, 3].

Typically, each renewable generator requires a DC-AC converter (inverter) to inject power into the grid [4, 5, 6]. In the basic approach, the inverter current synchronizes with the grid voltage (*i.e.* unit power factor), and the magnitude depends on the power generated by the source. Depending on the power of the renewable generator, inverters may be single-phase or three-phase. The latter is used for medium and high power applications, while single-phase inverters are preferred for low power generators.

Single-phase inverters have gained importance in the last years due to their application in microinverters [7, 8] and string inverters for residential and commercial applications [9, 10]. In particular, microinverters offer highpotential in the energy market due to the modularity, simple installation and high efficiency [11]. New technologies in semiconductors like GaN transistors, allow to manage low and medium power with higher switching frequencies, and reduced components sizes as well as better thermal and electrical performances [12]. The conventional full-bridge inverter, is probably the most common topology used in single-phase microinverters. It is formed by two legs connected in parallel to a DC bus, where each leg has two switches connected in series that operate in a complementary fashion. Major challenges with this approach are the avoidance of shoot-through current spikes due to the differences in the turn on and turn off time ratios of the switches. This problem is usually dealt with by introducing a delay in the control, at the cost of the voltage distortion. There are also, significant losses because of the reverse recovery currents passing through the protection diodes [9, 13].

As an alternative, the full-bridge dual-buck microinverter is currently investigated [14, 15, 16, 17]. This topology uses two complementary buck converters, each one operating in a semi-cycle of the grid voltage. Each buck converter has two switches, one commutes at high frequency and the other one remains active while the buck converter is operating. Some authors use two pairs of inductors [18, 19, 20, 21], while others reduce the number of inductors required to two or one [22, 23, 24]. In any case, using nonlinear modulation techniques is possible to deal with the shoot-through, reducing the switching losses while improving reliability [25].
In [22] the authors propose a grid-connected single-phase full-bridge dual-buck microinverter implemented with two inductors. The output of this converter is connected in parallel with a capacitor and the grid, which is represented by a sinusoidal voltage source. The study includes the development of a model to analyze the common mode current with and without a dead band in the transitions between the activation of one buck and the

deactivation of the other, analyzing the losses and evaluating the efficiency. The paper does not propose a control system, and instead the authors use a PWM modulation technique to generate the switching signals without providing details on the controller design. In addition, the proposed inverter only used a capacitor as an output filter, which reduces the inverter performance regarding the total harmonic distortion. In [21] the authors present a hysteretic controller for a dual-buck full-bridge microinverter with four inductors. The purpose is to feed a load with a sinusoidal voltage. Therefore, the authors propose an inner loop with a sliding mode controller for the current in the inductor, and an outer loop with a PI controller for the voltage in the output.

Regarding hysteresis control techniques, researchers focus on limiting high variation in the switching frequency by using fix or adaptive hysteretic bands[26, 27, 28, 29]. To minimize harmonics injected into the grid, filters *L*, *LC*, *LCL* are frequently used. Even though *LCL* filter increases the number of components, it is effective at lower switching frequencies and reduces size and cost. In [30], the authors presents a control technique for gridconnected inverter using a *LCL* filter, to improve the system stability, control performance, and harmonic suppression. In [31], researcher perform a comparison between a *L* filter and a *LCL* filter. The *L* filter has a marginal greater average life; however the *LCL* filter offers the best total harmonic distortion supression.

This paper presents an analytical and numerical study of a hysteresis control to regulate the current injected to the grid by a single-phase dual-buck inverter. The implementation uses two inductors and a *LC* filter. The analysis includes a mathematical model of the inverter and proposes a hysteresis controller of the inductor current. This study also provides guidelines for the selection of the hysteresis band and proposes a methodology to compute the dead band required for the transition between the positive and negative cycles of the grid voltage. A numerical validation through simulation presents the performance of the control and the dead band. The results also show the ability of the controller to operate for different magnitudes of the injected current.

2. Dual-buck DC-AC converter

The open loop operation of the converter can be understood as two individual buck converters working half cycle each in a complementary fashion [22, 32, 33].
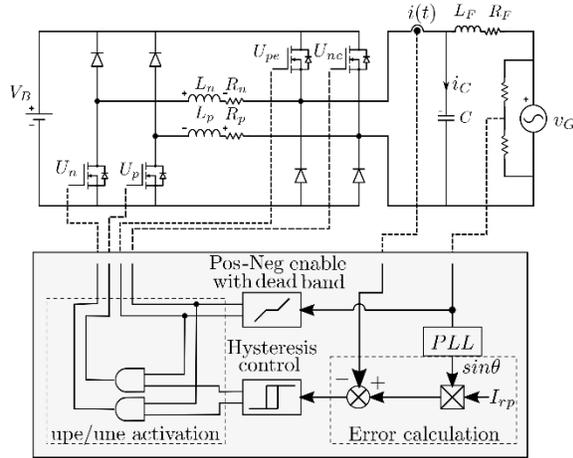
Figure 1. Dual-Buck schematics.

Figure 1 presents the schematics for an application where power from a generic DC source vB is used by the converter to inject active power into an AC grid vG defined as:

$$v_G(t) = V_p \sin(\omega\, t) \tag{1}$$

The solid state switches determine which converter is active through the control signals U_{pe}, $U_{pe} \in \{0, 1\}$ in such a way that only one switch is active at a particular time (*i.e.* $U_{pe} \cdot U_{ne} = 0$). This guarantees that L_p has positive current (i.*e.* $i(t) > 0$) on the positive semicycle of the sinusoidal reference, while L_n has negative current (*i.e.* $i(t) < 0$) on the negative semicycle. Finally, the control signals U_p, $U_n \in \{0, 1\}$ are available to perform the control task at a higher frequency. The dynamic equations for the converter can be written as follows:

$$\frac{di(t)}{dt} = \frac{1}{L_p}\Big(-R_p i(t) -\, v_C(t) +\, v_B\, U_p(t)\Big)$$
$$\frac{dv_C(t)}{dt} = \frac{1}{C}\Big(i(t) - i_F(t)\Big) \tag{2}$$
$$\frac{di_F(t)}{dt} = \frac{1}{L_F}\Big(v_C(t) - R_F i_F(t) - v_G(t)\Big)$$

with $U_{ne} = 0$, and $U_{pe} = 1$, and

$$\frac{di(t)}{dt} = \frac{1}{L_n}\Big(-R_n i(t) -\, v_C(t) +\, v_B\, U_n(t)\Big)$$
$$\frac{dv_C(t)}{dt} = \frac{1}{C}\Big(i(t) - i_F(t)\Big) \tag{3}$$
$$\frac{di_F(t)}{dt} = \frac{1}{L_F}\Big(v_C(t) - R_F i_F(t) - v_G(t)\Big)$$

with $U_{ne} = 1$, and $U_{pe} = 0$. The state variables are the current i in the inductance (L_p for the positive semicycle and L_n for the negative semicycle), the voltage v_C in the capacitor C and the current i_F in the inductance L_F.

3. Hysteresis Control

ROL Hysteresis control with fixed or adaptive bands have been widely studied in grid connected inverters [34, 35, 36]. Here, we propose a control task that can be stated through the design of an error surface:

$$e(t) =\, i_r - i(t) \tag{4}$$

where i_r is a reference current defined in (5), I_{rp} is the magnitude of the current injected into the grid and its its value is obtained from a higher-level controller, and ωt is obtained from a Phase-Locked Loop (PLL) control system, which tracks the grid frequency and phase:

$$i_r(t) =\, I_{rp} \sin \omega t \tag{5}$$

(5) The purpose of the control is to force the error in (4) to evolve within a hysteresis band of size H, define

$$\eta := \{e(t)|e(t)| - H \le 0\}$$

Let us define the control strategy where the control signals $U_p(t)$ and $U_n(t)$ change value whenever $e(t)$ reaches the boundaries of the hysteresis band η. This can be written as:
$$\partial\eta := \{e(t)|e(t)| = H\}$$

For simplicity, we will explain the rationale for the control strategy in the positive semi cycle taking advantage of the symmetries in the circuit for the negative semi cycle. Under the assumption that there is always a control action in the boundary, a suitable strategy would be to choose $U_p \in \{0, 1\}$ for two possible scenarios.

- $e(t) = H$. This implies that $i(t) < i_r(t)$, and the control switch must be activated setting $U_p=1$.
- $e(t) = H$. This implies that $i(t) > i_r(t)$, and the control switch must be activated setting $U_p=0$.

0. Unfortunately, the strategy described above, does not guarantee that the error will remain in the region η for the whole positive semi-cycle. Indeed, at every zero crossing of the reference current $i_r(t)$ the derivative $di(t)/dt$ vanishes for a particular value of $U_p(t)$ and $U_n(t)$. This conclusion can be drawn by evaluating the first equation of (2) when $i_r(t) \approx 0\ A$ and $v_G(t) \approx 0\ V$, which occurs at the same time because they are in phase. Therefore, the two possible values of $di(t)/dt$ for $U_p(t) = 1$ or $U_p(t) = 0$ are shown in (6) and (6), respectively. Those equations indicate that $i(t)$ is able to increase but not to decrease when $i_r(t) \approx 0\ A$ and $v_G(t) \approx 0\ V$, as consequence $e(t)$ does not evolve within the hysteresis band *H*.

$$\frac{di(t)}{dt}\bigg|_{U_p(t)=1} = \frac{v_B}{L_p}, \quad \frac{di(t)}{dt}\bigg|_{U_p(t)=0} = \frac{0}{L_p}, \quad (6)$$

Performing the same analysis for the negative semi-cycle, the values of $di(t)/dt$ for $U_n(t) = 1$ and $Un(t) = 0$ are shown in (7) and (7), respectively.

$$\frac{di(t)}{dt}\bigg|_{U_n(t)=1} = \frac{-v_B}{L_n}, \quad \frac{di(t)}{dt}\bigg|_{U_n(t)=0} = \frac{0}{L_n}, \quad (7)$$

The next subsection presents a complete mathematical analysis and design of a dead band near the zero-crossing of $i_r(t)$.

3.1. Dead band design

As an analytical tool, we use the average model where the switching control actions U_p and U_n can be described by an average model [37, 38], as follows:

$$\bar{U}_p(t) = \frac{1}{T}\int_t^{t+T} U_P(\tau)d\tau, \text{ and } \bar{U}_n(t) = \frac{1}{T}\int_t^{t+T} U_n(\tau)d\tau,$$

where T can be defined as a complete cycle of the control action. By doing so, it is possible to use the first dynamic equation from (2) and (3) to obtain an averaged control as:

$$\bar{U}_p(t) = \frac{1}{v_B}\left(L_p \frac{di_r(t)}{dt} + R_p\, i_r(t) + \bar{v}_C(t)\right)$$

$$\bar{U}_n(t) = -\frac{1}{v_B}\left(L_n \frac{di_r(t)}{dt} + R_n\, i_r(t) + \bar{v}_C(t)\right)$$

Where $\bar{v}_C = v_G(t) + R_F\, ir(t)$. Doing the substitution we have:

$$\bar{U}_p(t) = \frac{1}{v_B}\left(L_p \frac{di_r(t)}{dt} + R_p i_r(t) + v_G(t) + R_F\, i_r(t)\right)$$

$$\bar{U}_n(t) = -\frac{1}{v_B}\left(L_n \frac{di_r(t)}{dt} + R_n i_r(t) + v_G(t) + R_F\, i_r(t)\right)$$

Using (5) we obtain an exact expression for the average control action as:

$$\bar{U}_p(t) = A_p \sin(\omega t) + B_p \cos(\omega t)$$
$$\bar{U}_n(t) = A_n \sin(\omega t) + B_n \cos(\omega t)$$

where,

$$A_P = (V_P + 2I_{rp}R_P)/v_B \qquad B_P = I_{rp} L_P\, \omega/v_B$$
$$A_n = (V_P + 2I_{rp}R_n)/v_B \qquad B_n = -I_{rp} L_P\, \omega/v_B$$

Finally, using trigonometric identities we have:

$$\bar{U}_p(t) = C_p \sin(\omega t + \phi_p) \qquad (8)$$
$$\bar{U}_n(t) = C_n \sin(\omega t + \phi_n) \qquad (9)$$

where

$$C_P = \sqrt{A_P^2 + B_P^2}, \qquad \phi_P = tan^{-1}(A_P/B_P)$$
$$C_n = \sqrt{A_n^2 + B_n^2}, \qquad \phi_n = tan^{-1}(A_n/B_n) - \pi$$

Now, it is possible to compute the size of a dead band near the zero crossing of $v_G(t)$ using the angles φ_p and φ_n. Conditions in (8) and (9) show that $U_p \in [0, 1]$ if $\omega t \in [0, \pi-\varphi_p]$ and $U_n \in [0, 1]$ if $\omega t \in [\pi, 2\pi-\varphi_n]$. Figure 2 presents the computation of the average control actions $\bar{U}_p$ and $\bar{U}_n$ needed to achieve the tracking of a sinusoidal reference $i_r(t) = \sin(2\pi f_s\, t)$. It can be noticed that $U_p < 0$ for $\omega t \in [\pi - \varphi_p, \pi]$. In the positive semi-cycle, the dead band is calculated as the grid voltage when $\omega t = \pi-\varphi_p$ as $V_{dbp} = V_p \sin(\pi - \varphi_p)$. Similarly, in the negative semicycle the dead band can be defined as the grid voltage when $\omega t = 2\pi - \varphi_n$ as $V_{dbn} = V_p \sin(2\pi - \varphi_n)$. However, $|V_{dbp}| = |V_{dbn}|$ considering that $v_G(t)$ is sinusoidal; hence, the proposed dead band is defined at both sides of the point $v_G(t) = 0\ V$, i.e. the hysteresis controller does not operate when condition $|V_G| < V_{db}$ is met, where $V_{db} = |V_{dbp}| = |V_{dbn}|$ [39].
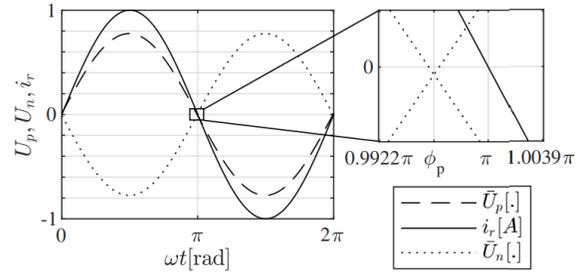

Figure 2. $\bar{u}_p(t)$ (dashed), $\bar{u}_n(t)$ (dotted) and $i_r(t)$ (continuous).

3.2. Maximum switching frequency

To determine the maximum switching frequency, we compute the shortest period T in the ripple of the error signal. Figure 3 shows conceptually the current. From (2), (4) and (5) it is possible to define the maximum slope of e(t) calculating its derivative term as shown in (10).

$$\frac{de(t)}{dt} = I_{rp}\omega cos(\omega t) + \frac{1}{L_p}(R_p i(t) + v_c(t) - v_B U_p(t)) \qquad (10)$$

Then, the rising and falling slopes of $e(t)$ are calculated from (10) assuming $i(t) \approx I_{rp} \sin(\omega t)$, $v_c \approx v_G(t) = V_p \sin(\omega t)$ and the the value of $U_p = \{0, 1\}$. i.e. when $U_p = 0$ the rise slope is:

$$\frac{de_{rise}(t)}{dt} = I_{rp}\omega cos(\omega t) + \frac{1}{L_p}(R_p I_{rp}\sin(\omega t) + V_p \sin(\omega t)) \qquad (11)$$

when $U_p = 1$, the falling slope is:

$$\frac{de_{fall}(t)}{dt} = I_{rp}\omega\cos(\omega t) + \frac{1}{L_p}(R_p I_{rp}\sin(\omega t) + v_G\sin(\omega t) - v_B) \quad (12)$$

The variation of the period T with time can be calculated as the time required by the error to increase from $-H$ to $+H$ during the rising slope, plus the time required by the error to reduce from $+H$ to $-H$ during the falling slope, as shown in (13).

$$T(t) = \frac{2H}{\frac{de_{rise}}{dt}} + \frac{2H}{\frac{de_{fall}}{dt}}, \quad F(t) = \frac{1}{\frac{2H}{\frac{de_{rise}}{dt}} + \frac{2H}{\frac{de_{fall}}{dt}}}, \quad (13)$$

From the definition of $F(t)$, it is clear that the switching frequency vary with the time according to $v_G(t)$ and $i_r(t)$. Figure 4 shows an example of the switching frequency of Up during the positive semi-cycle of $v_G(t)$ and $i_r(t)$ for the parameters given in Table 1. It can be observed that the $F(t)$ has two equal maximums ($F_{max} = 112.49$ kHz) and the minimum value is near 0 Hz. The behavior of the switching frequency for U_n is symmetric. It is worth noticing that F_{max} depends on the selection of H. Therefore, it is important to analyze the variation of the maximum frequency F_{max} for different values of H. Figure 5 shows an exponential growth of F_{max} for variations of H. This is a useful tool to define H considering the switching characteristics of the semiconductor devices. A similar analysis is carried on in [40] to design the size of the inductor according with the maximum frequency.
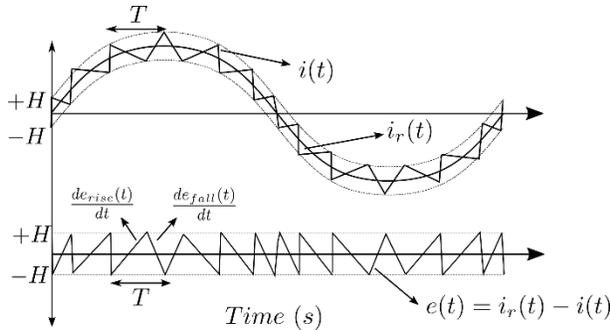

Figure 3. F$_{max}$ calculation.

3.3. Phase Lock Loop (PLL) implementation

A Phase Lock Loop simulink block to generate a normalized sinusoidal signal $v_r(t)$ in phase with $v_G(t)$, which is then used to generate the reference of the current control is presented in Figure 6. The PLL tracks the frequency and phase by using an internal frequency oscillator and a control system to adjusts the internal

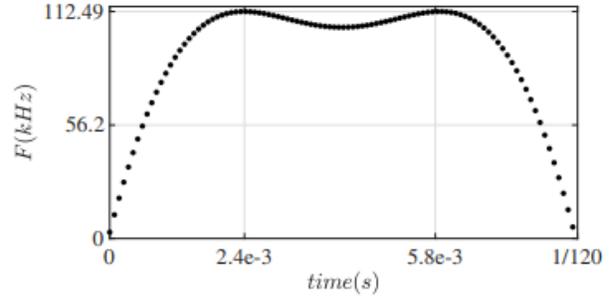oscillator frequency to keep the phases of $v_G(t)$ and $v_r(t)$ close to zero [41].

Figure 4. Switching frequency variation during the half positive semi-cycle for $H = 0.60$ mA
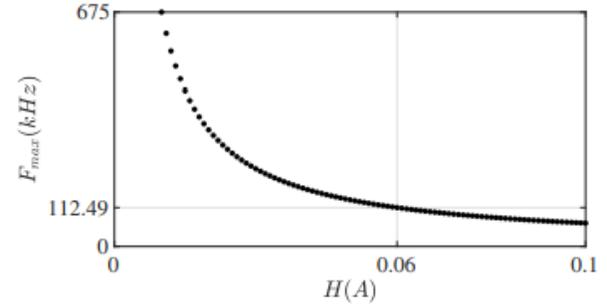

Figure 5. Maximum switching frequency variation with respect to the hysteresis value H.

Table 1. Microinverter specifications

Simulation specifications		
Inverter Parameters	**Symbols**	**Value**
Voltage DC Bus	V_{bus}	270 V
Grid Voltage amplitude	V_p	$\sqrt{2}$ 120 V
Grid Voltage frequency	f	60 Hz
Output Capacitor	C	0.22 μF
Dual-buck inductors	$L_n = L_p$	5 mH
Filter inductor	L_F	1 mH
Dual-buck L_p and L_n resist	$R_p = R_n$	0.93 Ω
Filter L_F resistance	R_f	0.01 Ω
Controller parameters	**Symbols**	**Value**
Hysteresis band	H	60 mA
Dead band voltage	V_{db}	9.4175 V
Max. freq. in Simulation	F_{max}	106.9kHz

Figure 7 shows the behavior of the PLL signal $v_r(t)$ under the limits in voltage and frequency allowed for the California Electric Rule No.21 [42]. A 5 % reduction in the magnitude of $v_G(t)$ is introduced in the second period (16 $mS > t > 33$ mS), in the third period a reduction from 60 Hz to 57 Hz in the grid frequency is performed (33 $mS > t > 50$ mS), and a 10 V and 1 kHz signal is added to $v_G(t)$ to simulate noise during the all simulation. It can be observed that $v_r(t)$ is in phase with the grid voltage even

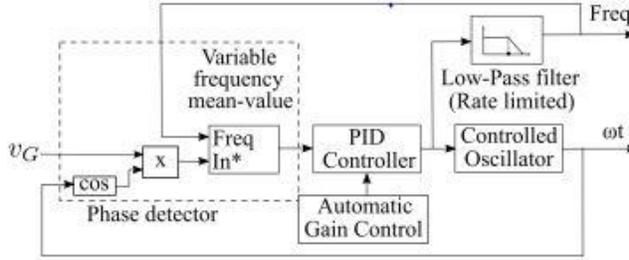in the presence of noise and changes in $v_G(t)$ magnitude and frequency.

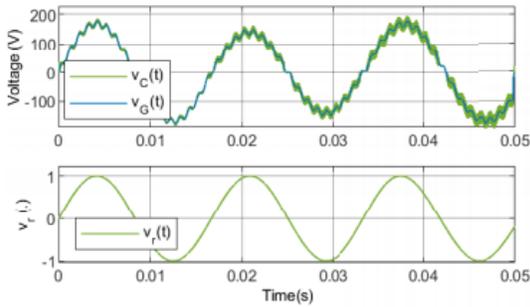Figure 6. Block diagram of Matlab/Simulink PLL operation.

Figure 7. PLL output ($v_r(t)$) under noise and variations of amplitude and frequency of $v_G(t)$. From top to bottom: first plot shows $v_G(t)$ and $v_C(t)$, and the second plot shows the PLL output $v_r(t)$.

4. Simulation results

The proposed hysteresis controller is implemented in Matlab/Simulink to evaluate its performance as shown in Figure 8. The circuital elements used to implement the gridconnected power converter are taken from Simscape/Power Systems library; while the hysteresis current controller is implemented by using just two comparators, an S-R flipflop, and a simple Matlab function that implements the dead band from $v_G(t)$ and V_{db}.

The controller implementation in Simulink is illustrated in Figure 9 and can be divided into five blocks: "positive/negative enable", "U_{pe}/U_{ne} activation", "PLL", "error calculation", and "hysteresis control". The first block compares the grid voltage ($v_G(t)$) with a fixed value (V_{db}) to determine which Buck is active and which is inactive by defining values of U_{pe} and U_{ne}; therefore, if $v_G(t) > V_{db}$, then $U_{pe} = 1$ and $U_{ne} = 0$, which means that the positive Buck is active and the negative one is inactive. Otherwise, if $v_G(t) < Vdb$, then $U_{pe} = 0$ and $U_{ne} = 1$. These signals (U_{pe} and U_{ne}) are used by "U_{pe}/U_{ne} activation" block to generate the boolean signals U_{pe} and U_{ne} required to activate the Mosfets S_{pe} and S_{ne},

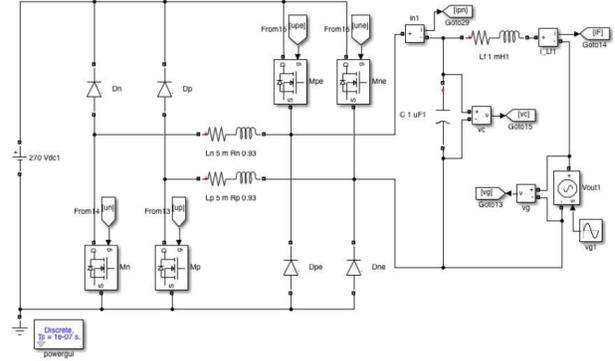respectively. Those boolean signals are generated with the AND blocks.

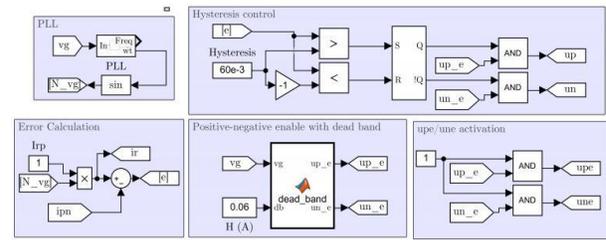Figure 8. Dual-Buck converter implemented in Simulink.

Figure 9. Hysteresis controller implemented in Simulink.

The PLL block generates a normalized sinusoidal waveform ($v_r(t)$) in phase with $v_G(t)$, which is multiplied by the scalar I_{rp} to generate $i_r(t)$. The Error calculation block evaluates the instantaneous error $e(t)$ in the current $i(t)$ with respect to the reference ($i_r(t)$), which is used by the Hysteresis control block. This block compares $e(t)$ with the hysteresis band H to determine if the high frequency switch turns on or off.

On the one hand, for the Buck that operates when $v_G(t) > V_{db}$, the hysteresis control operates as follows: if $e(t) > H$, then flip-flop is set to turn the switch on, and if $e(t) < -H$, then flipflop is reset to turn the switch off. On the other hand, for the Buck converter that operates when $v_G(t) < V_{db}$ the logic is the opposite. Therefore, it is enough to use the complement output of the flip-flop. At the output of the hysteresis control block, the AND functions enable the switching signal for the positive or negative Buck converter, by using U_{pe} and U_{ne}. Additionally, they also generate the Boolean signals U_p and U_n required to activate the high-frequency switches.

4.1. Control validation

The validation of the proposed controller is performed by generating a reference current $i_r(t)$ with different peak values: $I_{rp} = 1.0\ A$, $I_{rp} = 1.5\ A$ and $I_{rp} = 2.0\ A$. Moreover,

the parameters used in the simulations are introduced in Table 1. The main inverter variables for $I_{rp} = 1.0\ A$ are shown in Figure 10, where the top plot shows that $i(t)$ follows the reference $i_r(t)$ for the positive and negative semi-cycles. Such a plot also illustrates that the average value of the current injected to the grid ($i_F(t)$) follows $i_r(t)$.

The second plot introduces the capacitor voltage ($v_C(t)$) and the grid voltage ($v_G(t)$). It can be observed that the average voltage of $v_C(t)$ follows $v_G(t)$ for the positive and negative semi-cycles. Additionally, the third plot shows the switching signals U_p (green) and U_n (blue) that operate in the positive and negative semi-cycles, respectively. In this plot, it can be clearly identified the dead-band for the transition between the activation of one converter and the other in the middle of the voltage cycle. The last plot in Figure 10 introduces the error in the current $e(t)$ and the hysteresis band defined as $H = \pm 60$ mA.
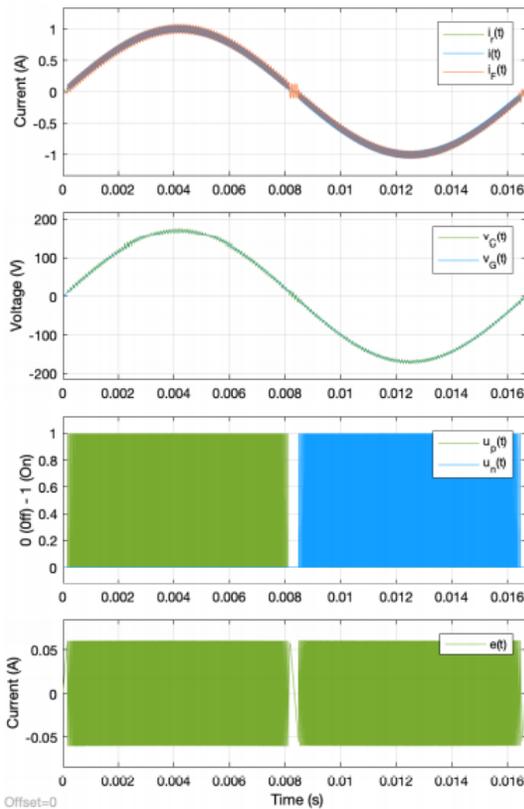

Figure 10. Main inverter variables for $I_{rp} = 1.0\ A$. From top to bottom: a) $i_r(t)$, $i(t)$, and $i_F(t)$, b) $v_C(t)$ and $v_G(t)$, c) $U_p(t)$ and $U_n(t)$, d) $e(t)$.

A zoom in of the variables introduced in Figure 10 is shown in Figure 11 to observe the behavior of the hysteresis controller and the transition between the positive and the negative Buck.

The dashed red lines illustrate the dead-band around $v_G(t) = 0\ V$ ($t = 8.33\ ms$ approximately). At the left of the dead-band the hysteresis controller turns a switch on (i.e. $U_p = 1$) when the error reaches the upper limit of the hysteresis band ($e(t) = 60_{mA}$), which means that $i(t)$ is below $i_r(t)$ and $i(t)$ increases with $U_p = 1$. Then, $i(t)$ continues increasing until the error reaches the lower limit ($e(t) = -60\ mA$) and the S_p is turned off to keep $e(t)$ within the hysteresis band. At the right of the dead-band, the controller operation is the opposite to the one described in the previous paragraph. When $e(t) = 60\ mA$ the controller turns S_n off to increase $i(t)$; while when $e(t) = -60\ mA$ the controller turns S_n on.
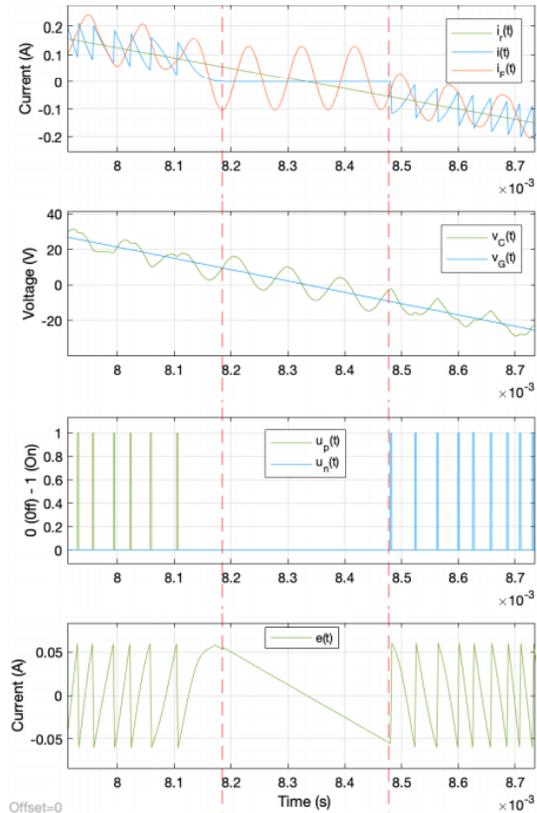

Figure 11. Zoom of the main inverter variables for $I_{rp} = 1.0\ A$. From top to bottom: first plot shows $i_r(t)$, $i(t)$, and $i_F(t)$, second plot shows $v_C(t)$ and $v_G(t)$, third plot shows $u_p(t)$ and $u_n(t)$, fourth plot $e(t)$.

Moreover, inside the dead band all the switches are off (i.e. $u_p = u_n = u_{pe} = u_{ne} = 0$); therefore, $i(t) = 0\ A$ and $e(t)$ remains within the hysteresis band. The proposed controller is also validated for step variations in the reference current as follows: $I_{rp} = 1$ for $0\ ms < t < 12.5\ ms$, $I_{rp} = 1.5$ for $12.5\ ms < t < 29.2\ ms$, and $I_{rp} = 2$ for $29.2\ ms < t < 45.8\ ms$. These particular times are selected to produce the step in I_{rp} at the minimum current. The main

inverter variables for the steps in I_{rp} are introduced in Figure 12.

It can be observed that $i(t)$ follows $i_r(t)$ even for steps in the amplitude of $i_r(t)$; nevertheless, the ripple in $i_F(t)$ considerably increases after each step in I_{rp}, which is also evidenced in the ripple of $v_C(t)$. Additionally, it is important to mention that $e(t)$ remains within the hysteresis band most of the time. The error leaves the hysteresis band when there are steps in I_{rp} and in the zero crossings; Nonetheless, it is worth noting that the controller brings $e(t)$ inside the hysteresis band in a short time.
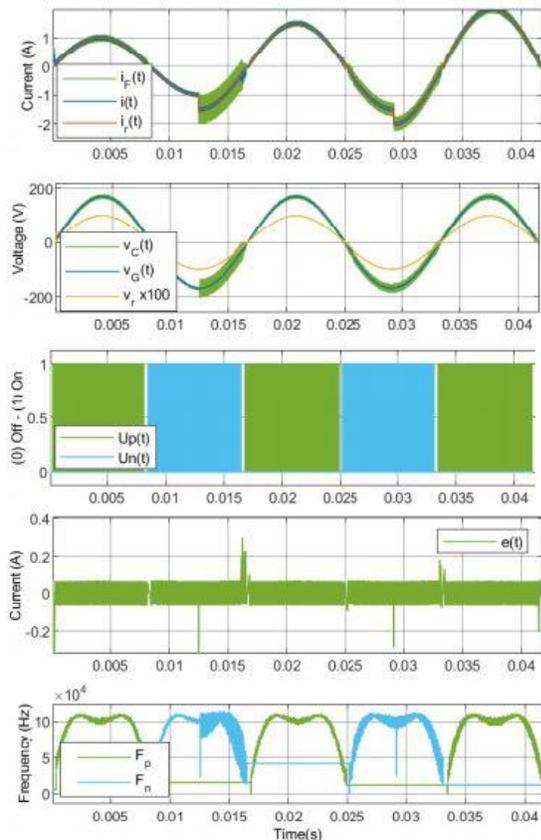

Figure 12. Main inverter variables with steps variations in I_{rp} ($I_{rp} = 1$ for 0 $ms < t < 12.5$ ms, $I_{rp} = 1.5$ for 12.5 $ms < t < 29.2$ ms, and $I_{rp} = 2$ for 29.2 $ms < t < 45.8$ ms). From top to bottom: first plot shows $i_r(t)$, $i(t)$, and $i_F(t)$, second plot shows $v_C(t)$ and $v_G(t)$, third plot shows $U_p(t)$ and $U_n(t)$, fourth plot $e(t)$, fifth plot shows the variation of the frequency commutation in time.

5. Conclusions

We have presented the hysteresis control of a dual-buck inverter for active power injection in a grid connected application. Using the dynamic equations for the error $e(t)$, we have designed a control strategy aiming to evolve

in a set $\eta \in [-H, H]$. Analytical conditions have been computed for the width of a dead band near the zero crossings of the AC reference $i_r(t)$. We have proposed an expression to compute an approximation of the instantaneous switching frequency and a numerical procedure to design the size of the hysteretic band H. In addition, numerical experiments for validation on the capacity of the control to synchronize with the grid, including perturbations in the voltage magnitude and frequency. Further simulations have shown, the performance of the dead-band and the hysteresis band to obtain a desired maximum switching frequency.

The control law proposed in this paper is easy to implement and does not require the exact model of the entire system, which make the controller suitable for different applications like photovoltaic systems, wind generators, battery chargers, UPSs, among others. The controller considers the nonlinear model of the inverter, which allows the tracking of the current reference for any operating condition. Nevertheless, the control does not warranty a correct current tracking during the dead band, which could produce reference tracking errors if there are disturbances during the dead-band. Another drawback related to the inverter topology is that the dead-band does not allow the injection of reactive power to the grid, since the phase difference between $i_r(t)$ and $v_G(t)$ increases the dead-band size. Additionally, the digital implementation requires the use of specialized microcontrollers with fast comparators, since the switching frequency varies exponentially reaching 500 kHz for $H = 10$ mA for the converter parameters used in simulations.

As future work, we propose the experimental validation of the controller and the spectral analysis of the injected power. More sophisticated control strategies might be developed using the analytical tools presented in this paper. It would be also interesting to include the proposed inverter and controller into a microgrid to analyze the performance of the proposed system in coordination with the microgrid control and the power quality injected in the connection point. Finally, we are working on the modification of the proposed controller and the inverter topology to inject reactive power.

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